A HIGH-FREQUENCY AND LOW-VOLTAGE CMOS AMPLIFIER

Elena DOICARU, Traian-Titi SERBAN
University of Craiova, Faculty of Automation, Computer Science and Electronics
Str. Lapus, Nr.5, 1100 Craiova, ROMANIA, e-mail: dmilena@electronics.ucv.ro

Abstract: In this paper is presented a CMOS amplifier with the following design specifications: the power supply voltage $V_{DD} - V_{SS} < 3\,\text{V}$, unity gain bandwidth $GB = 50\,\text{MHz}$, dc gain $A_0 = 80\,\text{dB}$, phase margin $\Phi_m \geq 50^o$, technology 1µm p-well CMOS, settling time t_s < 1µs, load $R_L // C_L = 10\,\text{K}\Omega // 10\,\text{pF}$ and minimum possible power consumption and area. The chosen topology for the amplifier was nested transconductance-capacitance compensation (NGCC) topology.

***Key words**: nested transconductance-capacitance compensation amplifier*

INTRODUCTION

The existing CMOS technologies provide ample opportunity to integrate entire systems on to a single integrated circuit. To date, the ability to integrate large digital systems has far outweighed the ability to integrate the analog systems. The greatest impediment to analog CMOS VLSI design has been the inability to provide consistent circuit performance over the broad range of requirements for signal gain, frequency response, phase response, delay, power and signal fidelity imposed by analog designs. More, as the power supply voltage for integrated circuits continues to scale down, the analog design in mixed signal environments is becoming more difficult and challenging. The main reason is that the threshold voltage is not expected to scale down proportionally to the supply voltage. To date, numerous analog signal processing systems (continuos time and sampled data) have been integrated for signals of interest below the low megahertz range. There remains a long-standing difficulty to integrate analog signal processing systems above this range.

The design specifications of the CMOS amplifier presented in this paper are: the power supply voltage $V_{DD} - V_{SS} < 3\,\text{V}$, unity gain bandwidth $GB = 50\,\text{MHz}$, dc gain $A_0 = 80\,\text{dB}$, phase margin $\Phi_m \geq 50^o$, technology 1 µm p-well CMOS, settling time t_s < 1µs, load $R_L // C_L = 10\,\text{K}\Omega // 10\,\text{pF}$ and minimum possible power consumption and area.

The chosen topology for the amplifier was dictated by these design specifications. The possible topologies suitable for high frequency are conventional cascode (CC), folder cascode (FC), mirrored cascode (MC), complementary folded cascode (CFC), nested Miller compensation multistage amplifier (NMC), multipath nested Miller compensation scheme (MNMC) and nested transconductance-capacitance compensation scheme (NGCC). But the conventional cascoding technique is not suitable for low-voltage application. Instead, the horizontal gain enhancement techniques (cascading) can be successful used.

The high value of specified dc gain can be obtains only by using three or more gain stages. But the amplifiers consisting of three or more gain stages cannot be frequency compensated by conventional means. A widespread compensation method like simple pole splitting is not capable of handling more than two poles. For this reason, high frequency bypass techniques are extensively used in high-frequency high-gain amplifiers. Several of these compensation techniques greatly worsen the settling time. But the requirement in this case is not critical so that of this point of view all NMC, MNMC and NGC topologies can be used. In designing a multistage amplifiers with multiple feedback loops stability is a delicate problem. Because of the complexity of the transfer function of the NMC and MNMC topologies, it is very difficult to derive stability conditions with reasonable complexity. For these reasons the NGCC topologies was prefer for implementation of amplifier.

To obtain high dc gain (>80 dB) from a multistage amplifier with simple (noncascode) gain stage, four stages will be typically required. The four stages NGCC topology used for this amplifier is shown in figure 1.

PROBLEM STATEMENT

In this section the transfer function and the stability conditions for NGCC amplifier will be derived.

Consider the four stages NGCC amplifier presented in figure 1. Assume that a capacitor C_L is connected at the output node and the output conductance at the output nods of the transconductance amplifiers G_{mi} is g_{oi}.

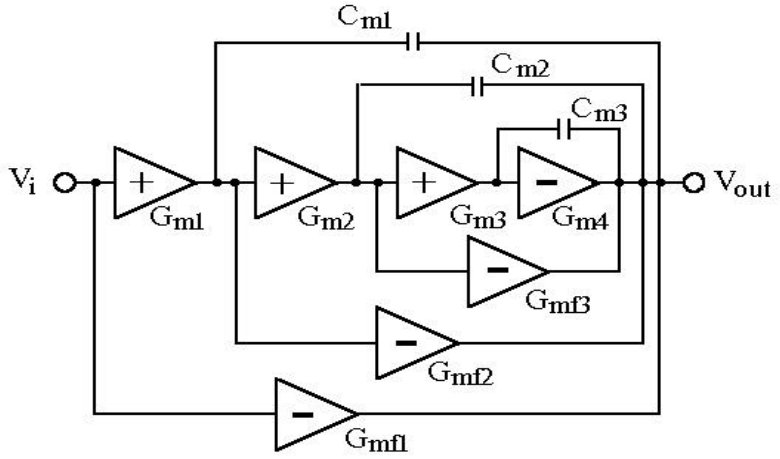

Figure 1. Conceptual NGCC topology of amplifier

Applying the Kirchoff low in the output nodes of the transconductances cells G_{mi} it is obtain the following expressions:

$$\begin{aligned}
&(g_{o4}+sC_L)\underline{V}_0 = -G_{mf1}\underline{V}_i - G_{mf2}\underline{V}_{01} - G_{mf3}\underline{V}_{02} - \\
&- G_{m4}\underline{V}_{03} + sC_{m3}(\underline{V}_{03}-\underline{V}_0) + sC_{m2}(\underline{V}_{02}-\underline{V}_0) + \\
&+ sC_{m1}(\underline{V}_{01}-\underline{V}_0) \\
&g_{o3}\underline{V}_{03} = G_{m3}\underline{V}_{02} - sC_{m3}(\underline{V}_{03}-\underline{V}_0) \\
&g_{o2}\underline{V}_{02} = G_{m2}\underline{V}_{01} - sC_{m2}(\underline{V}_{02}-\underline{V}_0) \\
&g_{o1}\underline{V}_{01} = G_{m1}\underline{V}_i - sC_{m1}(\underline{V}_{01}-\underline{V}_0)
\end{aligned} \tag{1}$$

Eliminating the $\underline{V}_{0i}$ variables from expressions (1), the amplifier transfer function it is obtain:

$$\frac{\underline{V}_0}{\underline{V}_i} = -\frac{s^3a_3 + s^2a_2 + sa_1 + a_0}{s^4b_4 + s^3b_3 + s^2b_2 + sb_1 + b_0}, \tag{2}$$

where the numerator parameters are:

$$\begin{aligned}
a_0 &= G_{m1}G_{m2}G_{m3}G_{m4} + g_{o1}g_{o2}g_{o3}G_{mf1} + \\
&+ g_{o2}g_{o3}G_{mf2}G_{m1} + g_{o3}G_{mf3}G_{m1}G_{m2} \\
&\cong G_{m1}G_{m2}G_{m3}G_{m4} \\
a_1 &= G_{m1}G_{m2}C_{m3}(G_{mf3}-G_{m3}) + \\
&+ G_{m1}g_{o3}C_{m2}(G_{mf2}-G_{m2}) + \\
&+ g_{o2}g_{o3}C_{m1}(G_{mf1}-G_{m1}) + G_{m1}g_{o2}G_{mf2}C_{m1} + \\
&+ g_{o1}G_{mf1}(C_{m2}g_{o3} + C_{m3}g_{o2}) \\
&\cong G_{m1}G_{m2}C_{m3}(G_{mf3}-G_{m3}) \\
a_2 &= G_{m1}C_{m2}C_{m3}(G_{mf2}-G_{m2}) + \\
&+ g_{o2}C_{m1}C_{m3}(G_{mf1}-G_{m1}) + \\
&+ g_{o3}C_{m1}C_{m2}(G_{mf1}-G_{m1}) + g_{o1}G_{mf1}C_{m2}C_{m3} \\
&\cong G_{m1}C_{m2}C_{m3}(G_{mf2}-G_{m2}) \\
a_3 &= G_{m1}C_{m2}C_{m3}(G_{mf1}-G_{m1})
\end{aligned} \tag{3}$$

and the denominator parameters are:

$$\begin{aligned}
b_0 &= g_{o1}g_{o2}g_{o3}g_{o4} \\
b_1 &= g_{o1}g_{o4}(g_{o2}C_{m3} + g_{o3}C_{m2}) + \\
&+ g_{o2}g_{o3}(g_{o4} + G_{mf2})C_{m1} + g_{o1}G_{m4}G_{m1}C_{m2} + \\
&+ g_{o3}G_{mf3}(G_{m2}C_{m1} + g_{o1}C_{m2}) + \\
&+ (\sum_{i=1}^{3} C_{mi} + C_L)g_{o1}g_{o2}g_{o3} + G_{m2}G_{m3}G_{m4}C_{m1}
\end{aligned} \tag{4}$$

$$\begin{aligned}
b_1 &\cong G_{m2}G_{m3}G_{mf4}C_{m1} \\
b_2 &= g_{o3}(G_{mf3}+g_{o4})C_{m1}C_{m2} + \\
&+ g_{o2}(G_{mf2}+g_{o4})C_{m1}C_{m3} + \\
&+ g_{o1}(G_{mf3}+g_{o4})C_{m2}C_{m3} + \\
&+ g_{o1}(G_{mf3}+g_{o4})C_{m2}C_{m3} + \\
&+ \left(\sum_{i\neq 3}^{3} C_{mi} + C_L\right)g_{o1}g_{o2}C_{m3} + \\
&+ \left(\sum_{i\neq 2}^{3} C_{mi} + C_L\right)g_{o1}g_{o3}C_{m2} + \\
&+ \left(\sum_{i=2}^{3} C_{mi} + C_L\right)g_{o2}g_{o3}C_{m1} + \\
&+ g_{o3}(G_{mf2}-G_{m2})C_{m1}C_{m2} + \\
&+ C_{m1}C_{m3}G_{m2}(G_{mf3}-G_{m3}) - \\
&- g_{o1}(G_{m4}-G_{m1})C_{m2}C_{m3} + G_{m4}G_{m3}C_{m1}C_{m2} \\
&\cong C_{m1}C_{m3}G_{m2}(G_{mf3}-G_{m3}) + G_{m4}G_{m3}C_{m1}C_{m2} \\
b_3 &= C_{m1}C_{m2}C_{m3}(G_{mf2}-G_{m2}) + \\
&+ C_{m1}C_{m2}C_{m3}(G_{mf3}-G_{m3}) + \\
&+ C_{m1}C_{m3}(C_{m2}+C_L)g_{o2} + \\
&+ C_{m1}C_{m2}(C_{m3}+C_L)g_{o3} + \\
&+ C_{m2}C_{m3}(C_{m1}+C_L)g_{o1} + G_{m4}C_{m1}C_{m2}C_{m3} \\
&\cong C_{m1}C_{m2}C_{m3}(G_{mf2}-G_{m2}) + \\
&+ C_{m1}C_{m2}C_{m3}(G_{mf3}-G_{m3}) + G_{m4}C_{m1}C_{m2}C_{m3} \\
b_4 &= C_LC_{m1}C_{m2}C_{m3}
\end{aligned} \tag{4}$$

The transfer function parameters contains same terms which have been ignored without losing accuracy because $g_{oi} << G_{mi}$ and $g_{oi} << G_{mfi}$. From simplified expressions of transfer functions parameter (3) and (4) it is observed that G_{mfi} will affect the zeros and the poles of the amplifier. By making $G_{mfi} = G_{mi}$ the expressions of parameters becomes:

$$\begin{aligned}
&a_0 \cong G_{m1}G_{m2}G_{m3}G_{m4}; a_1 = a_2 = a_3 = 0 \\
&b_0 = g_{o1}g_{o2}g_{o3}g_{o4}; b_1 \cong G_{m2}G_{m3}G_{mf4}C_{m1} \\
&b_2 \cong G_{m4}G_{m3}C_{m1}C_{m2} \\
&b_3 \cong G_{m4}C_{m1}C_{m2}C_{m3} \\
&b_4 = C_LC_{m1}C_{m2}C_{m3}
\end{aligned} \tag{5}$$

Now, will be introduced the following parameters:

$$A_i = \frac{G_{mi}}{g_{oi}}$$
$$f_i = \frac{G_{mi}}{C_{mi}}, i = \overline{1,3};\ f_4 = \frac{G_{m4}}{C_L} \quad (6)$$

which correspond to the low-frequency gain and to the cutoff frequency of the each stage.

With these parameters the transfer function becomes:

$$\frac{V_0}{V_i} = \frac{-A_0}{1 + \frac{sA_0}{f_1} + \frac{s^2 A_0}{f_1 f_2} + \frac{s^3 A_0}{f_1 f_2 f_3} + \frac{s^4 A_0}{f_1 f_2 f_3 f_4}} \quad (7)$$
$$A_0 = \prod_{i=1}^{4} A_i$$

Applying the Routh stability criterion on the closed-loop transfer function of the unity gain follower can derive the stability conditions of the amplifier:

$$f_4 > f_2$$
$$f_4 > f_2 \frac{1}{1 - f_1 / f_3} \quad (8)$$

In conformity with approximation procedure presented in (You 1997), (7) can be simplified to the form:

$$\frac{V_0}{V_i} = \frac{-A_0}{(1 + \frac{sA_0}{f_1})(1 + \frac{s}{f_2} + \frac{s^2}{f_2 f_3} + \frac{s^3 A_0}{f_2 f_3 f_4})} \quad (9)$$

if the dominant pole $p_1 = f_1 / A_0$ are relatively low comparatively with the others poles.
Using expression (9), and assuming that $f_1 = GB$, where GB is the gain-bandwidth product, and that $f_2 < f_3$, $f_2 < f_4$, it is obtained the expression of the phase margin Φ_m of amplifier:

$$\Phi_m = 90^o - arctg\left(\frac{GB}{f_2} \cdot \frac{1 - GB^2 / f_3 f_4}{1 - GB^2 / f_2 f_3}\right) \quad (10)$$

IMPLEMENTATION OF NGCC TOPOLOGY

The implementation of four-stage NGCC topology is presented in figure 2. The differential stage M1-M4 realizes the G_{m1} transconductance cell and the transistors M5-M7 realize the feedforward stage G_{mf1}. The transistor M8 that has M9-M10 active load implements the second Gm stage. The transistor M12 represents the feedforward stage Gmf2. Evidently the both transistors have the same sizes. The G_{m3} cell is realized by transistors M13 whit the active load M14-M15. The same size transistor that implements G_{mf3} is M17. The transistor M18 corresponds to the four transconductance cell.

It easy to see that all gain stages, other than the differential stage, can operate with a supply voltage of $V_P + 2V_{DSsat}$, where V_P is the cutoff voltage of transistors. The differential stage determines the supply voltage level of circuit. The voltage requirement for this stage is $V_P + 3V_{DSsat}$. The technology 1 µm p-well CMOS offers $V_{Pn} = 0.7\text{V}$, $|V_{Pp}| = 0.9\text{V}$ so that it is possible to adopt a supply voltage $V_{DD} - V_{SS} = 2\text{V}$.

The design procedure for amplifier begins with the determination of cutoff frequency stage parameters f_i. Plotting with MATLAB the normalized power, settling time and (10), with respect (8), it can obtain a design space for amplifier. The normalized power consumption is defined as:

$$p = \frac{P}{(V_{DD} - VSS) I_4} = \frac{(V_{DD} - VSS)\sum_{i=1}^{4} I_i}{(V_{DD} - VSS) I_4} = \sum_{i=1}^{4} \frac{I_i}{I_4} \quad (11)$$

where I_i represents the dc current of i-th stage.
Assuming a constant rapport $I_{D\Diamond} = I_D / (W / L)$ for all circuit transistors, in conformity with (Doicaru 1998) it is obtain a constant rapport g_{mi} / I_{Di}. But, as it is see from figure 2, the G_{mi} gain are proportional with g_m of amplifier circuit transistors. Hence we can rewritten the expression as $G_{mi} / I_i = x = ct.$ and the normalized power as:

$$p = 1 + \sum_{i=1}^{3} \frac{G_{mi}}{G_{m4}} = 1 + \sum_{i=1}^{3} \frac{C_{mi} f_i}{C_L f_4} = 1 + \sum_{i=1}^{3} \frac{\alpha_i f_i}{f_4} \quad (12)$$
$$C_{mi} = \alpha_i C_L$$

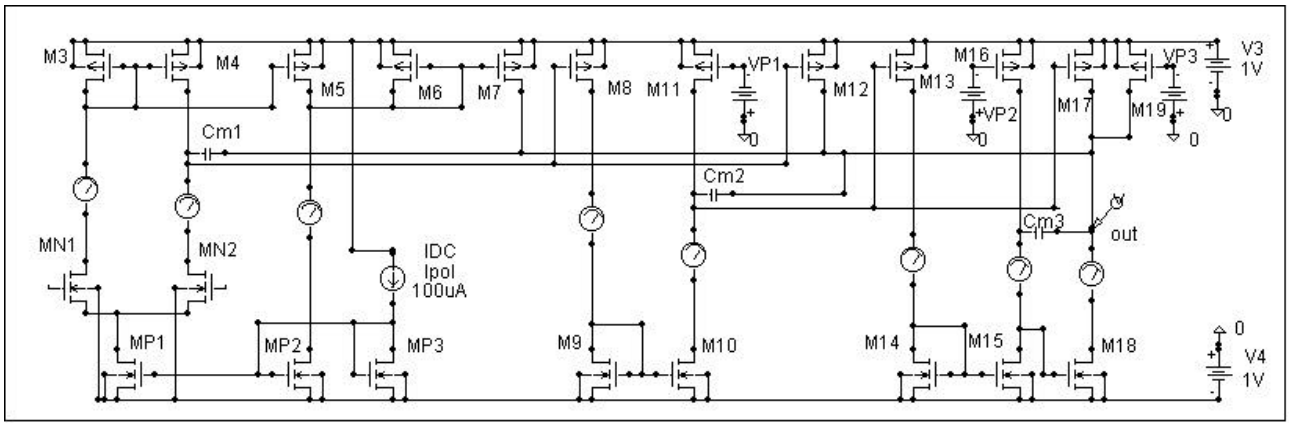

Figure 2. The implementation of NGCC topology

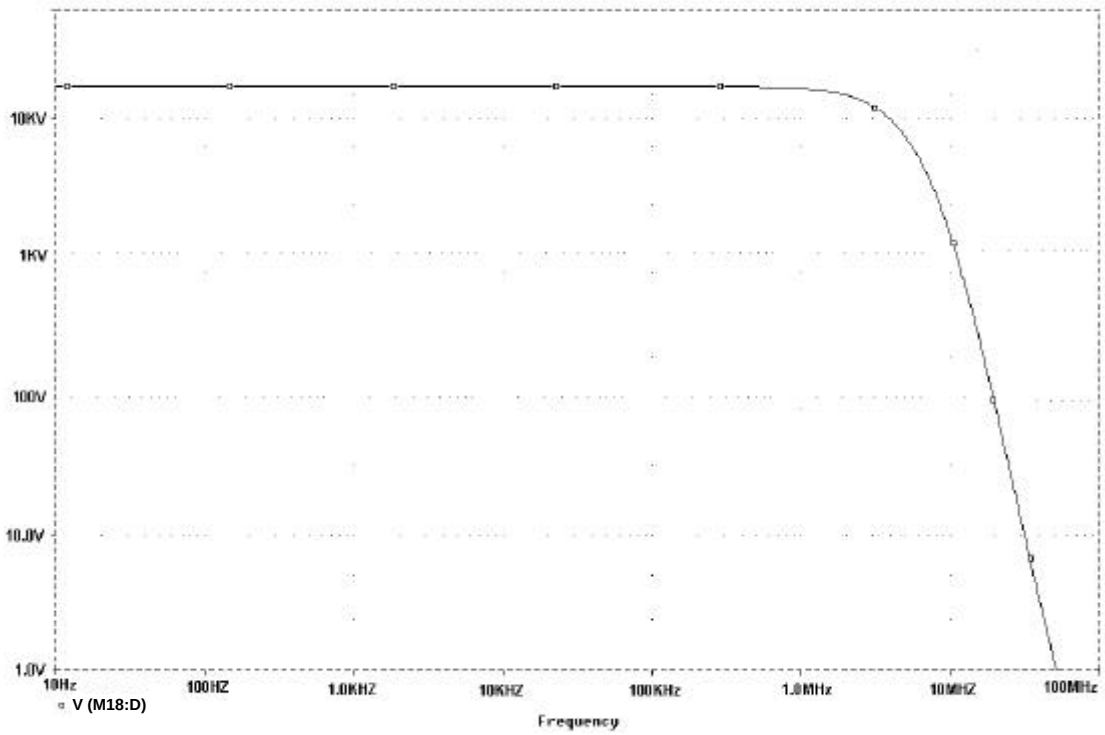

Figure 3. The amplitude-frequency characteristic of the amplifier

We used MATLAB plots obtained by the You in (You 1997) and in conformity with them we chose the cutoff frequency of each stage: $f_1 = GB = 50\text{MHz}$, $f_2 = 75\text{MHz}$, $f_3 = 150\text{MHz}$, $f_4 = 225\text{MHz}$. Next we have determined the transconductance of each stage: $G_{m1} = 2{,}5 \cdot 10^{-4}$, $G_{m2} = 3{,}75 \cdot 10^{-4}$, $G_{m3} = 7{,}5 \cdot 10^{-4}$, $G_{m4} = 22{,}5 \cdot 10^{-4}$. For simplicity we are choused $\alpha_i = 0{,}5, \quad i = \overline{1,3}$. The relations between G_{mi} and the transistors g_m are:

$$\begin{aligned} &g_{m1} = g_{m2} = G_{m1}/2; g_{m7} = G_{m1} \\ &g_{m8} = g_{m12} = G_{m2} \\ &g_{m13} = g_{m17} = G_{m3}; g_{m18} = G_{m4} \end{aligned} \tag{13}$$

The dc gain can be written as:

$$A_0 = \prod_{i=1}^{4} A_i = \frac{\prod_{i=1}^{4} G_{mi}}{\prod_{i=1}^{4} g_{oi}} = \frac{\prod_{i=1}^{4} (G_{mi}/I_i)}{\prod_{i=1}^{4} (g_{oi}/I_i)} = \frac{x^4}{\prod_{i=1}^{4} (g_{oi}/I_i)} \tag{14}$$

By written the conductance output of each stage as functions of output conductance of circuit transistors, written these conductance as functions of drain current and Early voltage and consider a variance of 7V/ μm for Early tension, we chose $x = 5$. Using the design plots (Doicaru 2000) and chose the same lengths of transistors of 2 μm we obtain the values for transistors sizes.

The table 1 summaries the PSPICE simulated parameters. Also the amplitude-frequency characteristic is shown in figure 3.

Table 1

Parameters	GB(MHz)	$\Phi_m(^o)$	A_0 (dB)
Calculated	50	50	80
Simulated	53	48	82

CONCLUSION

In this paper, a four stage amplifier with NGCC topology and his the design step and the results of SPICE simulation, that confirm the come true of design specification, has been presented. The topology is suitable for low voltage applications. The G_{mi}, $i=1 \div 3$, block of NGCC topology is realized using low-voltage non-inverting transconductance stages and G_{mfi} and G_{m4} of NGCC topology is realized using low-voltages transconductance inverting stages.

REFERENCES

Doicaru E., 1998, "A methodology for the Design of CMOS Analog Circuits", SINTES 9, Craiova.

Doicaru E., Dan C., 2000, "Low-noise wide band amplifier with inductive source", Proceeding of the 7th International Conference on Optimization of Electrical and Electronic Equipment, Brasov.

You F., Embabi S., 1997, "Multistage Amplifier Topologies with Nested G_m-C Compensation, Journal of Solid-State Circuits, vol.32, no. 12.